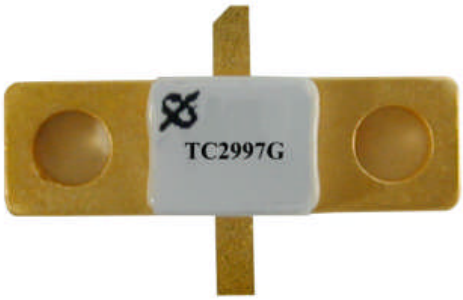
Preliminary

3.5 GHz 16 W Flange Ceramic Packaged GaAs Power FETs

FEATURES

- 16 W Typical Power at 3.5 GHz
- 9 dB Typical Linear Power Gain at 3.5 GHz
- High Linearity: IP3 = 52 dBm Typical
- High Power Added Efficiency: Nominal PAE of 37 %
- 100 % DC and RF Tested
- Flange Ceramic Package
- Suitable for WiMax and WLL applications

PHOTO ENLARGEMENT



DESCRIPTION

The TC2997G is a packaged Pseudomorphic High Electron Mobility Transistor (PHEMT) power transistor. The flange ceramic package provides the best thermal conductivity for the GaAs FET. All devices are 100% DC and RF tested to assure consistent quality. Typical applications include high dynamic range power amplifier for commercial applications.

ELECTRICAL SPECIFICATIONS

Symbol	CONDITIONS	MIN	TYP	MAX	UNIT
P_{1dB}	Output Power at 1dB Gain Compression Point, Vd = 10V, Id = 4A, f=3.4 – 3.6GHz	41.5	42.5		dBm
G_L	Linear Power Gain Vd = 10V, Id = 4A, f=3.4 – 3.6GHz	8	9		dB
IP3	Intercept Point of the 3rd-order Intermodulation, Vd = 10V, Id = 4A, f=3.4 – 3.6GHz, *P_{SCL} = 32 dBm		52		dBm
PAE	Power Added Efficiency at 1dB Compression Power		37		%
I_{DSS}	Saturated Drain-Source Current at V_{DS} = 2 V, V_{GS} = 0 V		18.75		A
g_m	Transconductance at V_{DS} = 2 V, V_{GS} = 0 V		13500		mS
V_P	Pinch-off Voltage at V_{DS} = 2 V, I_D = 60 mA		-1.7		Volts
BV_{DGO}	Drain-Gate Breakdown Voltage at I_{DGO} =15 mA	20	22		Volts
R_{th}	Thermal Resistance		0.6		°C/W

***P_{SCL}: Output Power of Single Carrier Level, delta frequency=5MHz.**

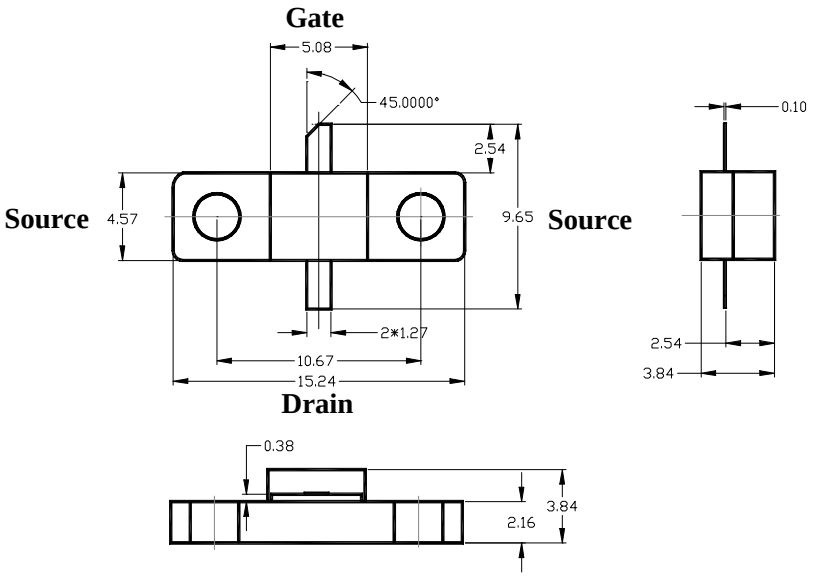
ABSOLUTE MAXIMUM RATINGS at 25 °C

Symbol	Parameter	Rating
V_{DS}	Drain-Source Voltage	12 V
V_{GS}	Gate-Source Voltage	-5 V
I_{DS}	Drain Current	I_{DSS}
P_{in}	RF Input Power, CW	37.5 dBm
P_T	Continuous Dissipation	150 W
T_{CH}	Channel Temperature	175 °C
T_{STG}	Storage Temperature	- 65 °C to +175 °C

HANDLING PRECAUTIONS:

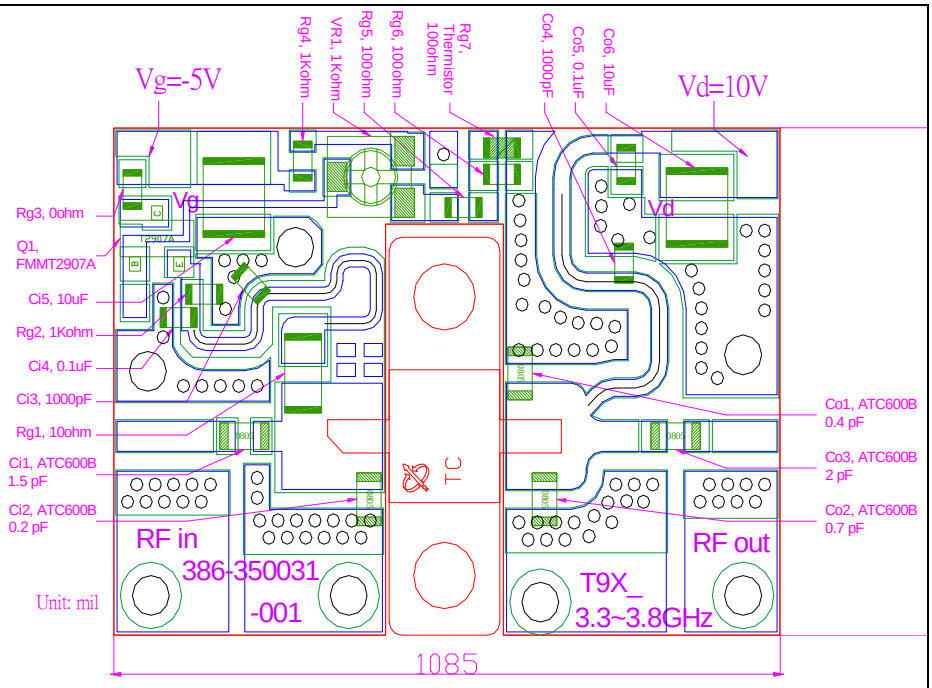
The user must operate in a clean, dry environment. Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. The static discharge must be less than 300V.

FLANGE PACKAGE OUTLINE (in mm)



EVALUATION BOARD

PCB Material: RO4003
ER = 3.38
Thickness = 20 mil
Unit: mil



Evaluation Board Parts List

Qt'y	Description	Reference Designator	Manufacturer	Inventory ID
1	Chip resistor (1206) 10Ω±5%	Rg1		
2	Chip resistor (0603) 1KΩ±5%	Rg2, Rg4		
1	Chip resistor (0603) 0Ω±5%	Rg3		
2	Chip resistor (0603) 100Ω±5%	Rg5, Rg6		
1	Thermistor (0402) 100Ω ±5%	Rg7		
1	SMT Trimmer Potentiometers (3.0*3.0mm) 1KΩ	VR1		
1	PNP, FMMT2907A (SOT-23)	Q1		
2	Chip CAP (0603) 1000PF±10%	Ci3, Co4	Murata	GRM39X7R102K50V
2	Chip CAP (0603) 0.1μF±20%	Ci4, Co5	Murata	GRM39Y5V104Z25V
2	Chip CAP (1210) 10μF±20% or (1206) 10μF±20%)	Ci5, Co6	Murata	GRM42-6Y5V106Z25V or GRM31CF5E106ZA01L
1	Chip CAP (0805) 1.5PF±0.1PF	Ci1	American Technical Ceramics	ATC 600F1R5BT250 WVDC
1	Chip CAP (0805) 0.2PF±0.1PF	Ci2	American Technical Ceramics	ATC 600F0R2BT250 WVDC
1	Chip CAP (0805) 0.4PF±0.1PF	Co1	American Technical Ceramics	ATC 600F0R4BT250 WVDC
1	Chip CAP (0805) 0.7PF±0.1PF	Co2	American Technical Ceramics	ATC 600F0R7BT250 WVDC
1	Chip CAP (0805) 2PF±0.1PF	Co3	American Technical Ceramics	ATC 600F2R0BT250 WVDC

Application Note:

High power FET turn on procedure

For evaluating or operating the high power FET, following turn-on and turn-off procedures are highly recommended to avoid the device oscillations or burnout.

Turn-on Procedure:

1.The input and output of the device must connect to 50ohm.
2.ESD protection.
3.Vd must connect to external “Regulated Circuit” with a DC regulator included, as similar as the idea shown herewith.
4.Voltage spike protection on input and output DC biasing is recommended.
5.Vgs set to -3V.
6.Open the output DC biasing (Vds).
7.Increase Vgs to get Idsq, quiescent drain current.
8.Turn on the RF driver.

Turn-off Procedure:

1.Turn off the RF driver.
2.Vg set to -3V.
3.Turn off Vd.
4.Turn off Vg.